

**IN THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:

generating command signals [[for]] to access[[ing]] an integrated circuit component;

accessing data signals [[for]] to convey[[ing]] data for the integrated circuit component;

accessing sampling signals [[for]] to control[[ing]] [[the]] sampling of the data signals; and

~~for both data write transactions and data read transactions, automatically adjusting a phase relationship between systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to calibrate operation of to determine a valid operation range of the integrated circuit device, wherein the automatic adjusting is free of user input valid operation range includes an optimal operation point for the integrated circuit device.~~

2. (Currently Amended) The method of claim 1, wherein the integrated circuit device [[is]] comprises a DRAM component.

3. (Currently Amended) The method of claim 2, wherein the adjusting of the phase relationship said altering is performed by a memory controller coupled to the DRAM component.

4. (Currently Amended) The method of claim 2, wherein the DRAM component [[is]] comprises a DDR DRAM component.

5. (Currently Amended) The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component.

6. (Currently Amended) The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component.

7. (Currently Amended) A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:

a controller configured to [[for]] generate[[ing]] command signals for accessing an integrated circuit component;

a delay calibrator integrated within the controller and configured to access data signals conveying data for the integrated circuit device and to access sampling signals for controlling [[the]] sampling of the data signals, and for both data write transactions and data read transactions, wherein the delay calibrator is further configured to automatically adjust a phase relationship between the command signals, the data signals, and the sampling signals to calibrate operation of the integrated circuit device, without requiring a valid initial operating point to exist within the specified operating parameters for the integrated circuit device, and wherein the automatic adjusting is free of user input systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device; and wherein the valid operation range includes an optimal operation point for the integrated circuit device.

8. (Currently Amended) The method system of claim 7, wherein the integrated circuit device [[is]] comprises a DRAM component.

9. (Currently Amended) The method system of claim 8, wherein the DRAM component [[is]] comprises a DDR DRAM component.

10. (Currently Amended) The method system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

11. (Currently Amended) The method system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

12. (Currently Amended) In a memory controller, a method for finding an operating mode for a DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DRAM component, the method comprising:

generating command signals [[for]] to access[[ing]] a DRAM component; accessing data signals [[for]] to convey[[ing]] data for the DRAM component; accessing sampling signals [[for]] to control[[ling]] [[the]] sampling of the data signals; and

~~for both data write transactions and data read transactions, automatically systematically altering a phase relationship between a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a[[n]] valid operating mode range of the DRAM component, without requiring a valid initial operating point to exist within the specified operating parameters for the DRAM component, and wherein the automatic altering is free of user input.~~

13. (Currently Amended) The method of claim 12, further comprising: performing a coarse calibration by altering the phase relationship the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the

sampling signals in accordance with a large step interval to [[find]] determine if the valid operating [[mode]] range of the DRAM component exists; and

if the valid operating range exists, then performing a fine calibration by altering the phase relationship the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal optimize the operating mode of the DRAM component.

14. (Currently Amended) The method of claim 13, further comprising[:]:  
configuring the memory controller to operate [[with]] the DRAM component in accordance with an the optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

15. (Currently Amended) The method of claim 12, wherein the DRAM component [[is]] comprises a DDR DRAM component.

16. (Original) The method of claim 15, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component.

17. (Original) The method of claim 16, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component.

18. (Currently Amended) A computer-readable media having stored thereon, computer-executable instructions that, if executed by a processor, cause the processor to perform a method for finding an operating mode for a DDR DRAM component by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the media storing computer readable code which when executed by a memory controller causes the memory controller to implement a the method comprising:

generating command signals [[for]] to access[[ing]] a DDR DRAM component;  
accessing DQ signals [[for]] to convey[[ing]] DQ signals for the DDR DRAM component;  
accessing DQS signals [[for]] to control[[ing]] [[the]] sampling of the DQ signals;  
and

~~for both data write transactions and data read transactions, automatically systematically altering a phase relationship between a phase shift of the command signals, a phase shift of the DQ signals, and a phase shift of the DQS signals to determine a[[n]] valid operating mode range of the DDR DRAM component, without requiring a valid initial operating point within the specified operating parameters for the DRAM component.~~

19. (Currently Amended) The computer-readable media of claim 18, wherein the method further comprising comprises:

performing a coarse calibration by altering the phase relationship the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a large step interval to find if the valid operating [[mode]] range of the DDR DRAM component exists; and

if the valid operating range exists, then performing a fine calibration by altering the phase relationship the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals in accordance with a small step interval to identify an optimal optimize the operating mode of the DDR DRAM component.

20. (Currently Amended) The computer-readable media of claim 19, wherein the method further comprising: comprises configuring the memory controller to operate [[with]] the DRAM component in-accordance with an the optimal operating mode, wherein the optimal operating mode is determined via the fine calibration.

21. (Cancelled)

22. (Currently Amended) In a memory controller, a method for finding an operating mode for a DDR DRAM component coupled to a PCB (printed circuit board) by altering intra-cycle timing relationships between command signals, data signals, and sampling signals for the DDR DRAM component, the method comprising:

generating command signals [[for]] to access[[ing]] a DDR DRAM component;

accessing data signals [[for]] to convey[[ing]] data for the DDR DRAM component;

accessing sampling signals [[for]] to control[[ling]] [[the]] sampling of the data signals; and

for both data write transactions and data read transactions, automatically systematically altering a phase relationship between a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals transmitted via a PCB to determine a[[n]] valid operating mode range of the DDR DRAM component, wherein the DDR DRAM component is inoperable at specified operating parameters, and wherein said automatic altering is performed free of user input.

23. (Canceled)

24. (Canceled))

25. (New) The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase.

26. (New) The method of claim 13, wherein said performing a fine calibration

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

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**Page 10**

Dkt: TRAN-P156

comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.